Techno India Batanagar
Computer Science and Engineering

Model Questions

Subject Name: Computer Architecture **Subject Code**: CS 403

Multiple Choice Type Questions

1. SIMD represents an organization that _____.
   i. refers to a computer system capable of processing several programs at the same time
   ii. represents organization of single computer containing a control unit, processor unit and a memory unit.
   iii. includes many processing units under the supervision of a common control unit
   iv. none of the above.

2. Floating point representation is used to store
   i. Boolean values
   ii. whole numbers
   iii. real integers
   iv. integers

3. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cyclesrequired for transfer stayed the same what would the bandwidth of the bus?
   i. 1 Megabyte/sec
   ii. 4 Megabytes/sec
   iii. 8 Megabytes/sec
   iv. 2 Megabytes/sec

4. Assembly language
   i. uses alphabetic codes in place of binary numbers used in machine language
   ii. is the easiest language to write programs
   iii. need not be translated into machine language
   iv. None of these

5. In 32-bit addressing mode, address field is either 1 byte or
   i. 2 bytes
   ii. 3 bytes
   iii. 4 bytes
   iv. 5 bytes

6. Maximum no of directly addressable locations in the memory of processor having 10 bits wide control bus,20 bits address bus,8-bit data bus is
   i. 1k
   ii. 2k
   iii. 1M
   iv. none of these

7. One of advantage of MIPS 16 and Thumb is: instruction caches acting as if they are about
   i. 10% larger
   ii. 25% larger
   iii. 30% larger
   iv. 40% larger

8. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .
   i. Pipe-lining
   ii. Super-scaling
   iii. parallel Computation
   iv. None of these

9. To extend the connectivity of the processor bus we use _____ .
   i. SCSI bus
   ii. PCI bus
   iii. Multiple bus
   iv. Controllers

10. One that is used to allocate local variables is
   i. Queue
   ii. Stack
   iii. Registers
   iv. Banks

11. Vector architectures are operated on vectors of
   i. Memory
   ii. Data
   iii. Registers
   iv. Graph coloring

12. Graph coloring gives best results, when there are at-least
   i. 16 general-purpose registers
   ii. 24 general-purpose registers
   iii. 32 general-purpose registers
   iv. 64 general-purpose registers

13. In Reverse Polish notation, expression A*B+C*D is written as
   i. AB*CD*+
   ii. A*BCD*+
   iii. AB*CD+*
   iv. A*B*CD+

14. Compilers usually chooses which procedure calls has to be expanded inline before knowing size of procedure, that is being called, stated problem is known as
   i. Caller saving
   ii. Callee saving
   iii. Phase-ordering problem
   iv. All above

15. IBM developed a bus standard for their line of computers PC AT called _____ .
    i. M-bus
    ii. IB bus
    iii. ISA
    iv. None of these

16. The bus used to connect the monitor to the CPU is _____ .
    i. SCSI bus
    ii. PCI bus
    iii. Rambus
    iv. Memory bus

17. The ultimate goal of a compiler is to,
    i. Reduce the size of the object code.
    ii. Reduce the clock cycles for a programming task.
    iii. Be able to detect even the smallest of errors.
    iv. Be versatile.

18. Operation is normally specified in one field, known as
    i. Oprand
    ii. Opcode
    iii. Operation
    iv. Instruction count

19. Length of 80x86 instructions can vary between
    i. 1 to 10 bytes
    ii. 2 to 8 bytes
    iii. 2 to 17 bytes
    iv. 1 to 17 bytes

20. Optimization, known as basic block, by compiler people is
    i. Global common sub-expression elimination
    ii. High-level optimizations
    iii. Local optimizations
    iv. Global optimizations

21. Procedure when call procedure that has been called, saving registers it wants for using, when caller has been left unrestrained, is known as
    i. Caller saving
    ii. Calls
    iii. Callee saving
    iv. Jumps

22. When Performing a looping operation, the instruction gets stored in the _____ .
    i. Cache
    ii. Registers
    iii. System stack
    iv. System Heap

23. The clock rate of the processor can be improved by,
    i. By using overclocking method

ii. Improving the IC technology of the logic circuits
iii. Reducing the amount of processing done in one step
iv. All of the above

24. When call procedure saving registers which it wants to be preserved to access even after call, is referred to as
    i. Caller saving
    ii. Callee saving
    iii. Calls
    iv. Jumps

25. Replacing instances of a variable, to which a constant is assigned with constant, is referred as
    i. Global common sub-expression elimination
    ii. Stack height reduction
    iii. Heap
    iv. Constant propagation

26. Optimization: finding two examples of an expression, computing same value and saving value of 1st computation in a temporary variable, is referred as
    i. Global common sub-expression elimination
    ii. Global sub-expression elimination
    iii. Global elimination
    iv. Sub-expression elimination

27. Register allocation algorithms are particularly based on technique, named as
    i. Low-level optimizations
    ii. High-level optimizations
    iii. Phase-ordering problem
    iv. Graph coloring

28. Specified telling that what addressing mode will be used for accessing operand, is called
    i. Address specified
    ii. Binary-coded decimal
    iii. Unpacking
    iv. Packed decimal

29. Unit is used for allocating dynamic objects which do not adhere to stack discipline is
    i. Queue
    ii. Stack
    iii. Heap
    iv. Banks

30. During the execution of the instructions, a copy of the instructions is placed in the _____ .
    i. Register
    ii. RAM
    iii. System heap
    iv. Cache

31. The main virtue for using single Bus structure is
    i. Cost effective connectivity and speed

ii. Fast data transfers
iii. Cost effective connectivity and ease of attaching peripheral devices
iv. None of these

32. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

i. A
ii. B
iii. Both take the same time
iv. Insufficient information

33. _____ are used to overcome the difference in data transfer speeds of various devices.
i. Bridge circuits
ii. Speed enhancing circuitry
iii. Buffer registers
iv. Multiple Buses

34. An optimizing Compiler does,
i. Better compilation of the given piece of code.
ii. Takes advantage of the type of processor and reduces its process time.
iii. Does better memory management.
iv. Both a and c

35. _____ register Connected to the Processor bus is a single-way transfer capable
i. Temp
ii. PC
iii. Z
iv. IR

36. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution ?
i. Super-scalar
ii. ISA
iii. ANSA
iv. All of the above

37. In multiple Bus organization, the registers are collectively placed and referred as _____ .
i. Register file
ii. Set registers
iii. Register Block
iv. Map registers

38. The main advantage of multiple bus organisation over single bus is,
i. Increase in size of the registers
ii. Reduction in the number of cycles for execution
iii. Better Connectivity
iv. None of these

39. As of 2000, the reference system to find the performance of a system is _____ .
i. None of these
ii. Ultra SPARC 10
iii. SUN II

iv. SUN SPARC

40. The ISA standard Buses are used to connect,
    i. A GPU and processor
    ii. B RAM and processor
    iii. C CD/DVD drives and Processor
    iv. D Hard-disk and Processor

41. SPEC stands for,
    i. Standard Performance Evaluation Code.
    ii. Standard Processing Enhancement Corporation.
    iii. System Processing Enhancing Code.
    iv. System Performance Evaluation Corporation.

42. The ascending order or a data Hierarchy is
    i. bytes - bit- field - record - file - database
    ii. bit - bytes - record - field - file - database
    iii. bytes -bit - record - field - file - database
    iv. bit - bytes - fields - record - file - database

43. In immediate addressing the operand is placed
    i. after OP code in the instruction
    ii. in memory
    iii. in stack
    iv. in the CPU register

44. How many address lines are needed to address each memory locations in a 2048 x 4 memory chip?
    i. 8
    ii. 10
    iii. 11
    iv. 12

45. A computer program that converts an entire program into machine language at one time is called a/an
    i. simulator
    ii. interpreter
    iii. commander
    iv. compiler

46. Interrupts which are initiated by an I/O drive are
    i. internal
    ii. external
    iii. software
    iv. all of above

47. When the RET instruction at the end of subroutine is executed,
    i. the memory address of the RET instruction is transferred to the program counter
    ii. the information where the stack is iniatialized is transferred to the stack pointer
    iii. two data bytes stored in the top two locations of the stack are transferred to the stack pointer
    iv. two data bytes stored in the top two locations of the stack are transferred to the program counter

48. A microporgram is sequencer perform the operation
    i. read
    ii. read and execute
    iii. execute

iv. write

49. The ALU and control unit of most of the microcomputers are combined and manufacture on a single silicon chip. What is it called?
    i. microprocessor
    ii. ALU
    iii. Mono-chip
    iv. control unit

50. Microprocessor 8085 can address location upto
    i. 32K
    ii. 128K
    iii. 64K
    iv. 1M

51. A first goal of compiler writer
    i. Correctness
    ii. Fast performance
    iii. Callee saving
    iv. Data dependence

52. Optimizations on sources with output leading to later optimization passes are known as
    i. Low-level optimizations
    ii. High-level optimizations
    iii. Local optimizations
    iv. Global optimizations

53. CPU gets the address of next instruction to be processed from
    i. Instruction registers
    ii. Index register
    iii. Program counter
    iv. none of these

54. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to
    i. the time it takes for the platter to make a full rotation
    ii. the time it takes for the read-write head to move into position over the appropriate track
    iii. the time it takes for the platter to rotate the correct sector under the head
    iv. none of the above

55. The addressing mode used in an instruction of the form ADD X Y, is
    i. Absolute
    ii. indirect
    iii. index
    iv. none of these

56. If no node having a copy of a cache block, this technique is known as
    i. Uniform memory access
    ii. Cached
    iii. Un-cached
    iv. Commit

57. When home node being local node, copies may exist in a third node, called
    i. Home node

ii. Guest node
iii. Remote node
iv. Host node

58. Alternative way of a snooping-based coherence protocol, is called a
    i. Memory protocol
    ii. Directory protocol
    iii. Register protocol
    iv. None of above

59. Requesting node sending requested data starting from memory, and requestor which has made only sharing node, known as
    i. Write miss
    ii. Write node
    iii. Read miss
    iv. Read node