Question Paper Details					
Course	**Stream**	**Semester**	**Subject**	**Paper Code**	**Chapter**
B.TECH	**ECE**	**4th**	**Digital Electronics & Integrated Circuits**	**EC-402**	**1 Data and number systems, Boolean algebra, Various Logic gates**

Paper Setter Details			
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MCQ [Type-1] **[Maximum marks: 1]**

1. Find the Decimal number representation of $(101101.10101)_2$
   a) 42.565 b)45.6562 c) 41.625 d) 49.5
2. Convert $(13.65625)_{10}$ to binary
   a)1010.1010 b) 11111.01010 c)1101.10101 d) none
3. Convert $(627.45)_8$ into its equivalent decimal number.
   a)470.75 b) 407.57 c) 704.57 d) 704.75
4. Convert $(387.51)_{10}$ into octal
   a)603.4631 b) 603.1364 c)306.1364 d)306.4631
5. Find the equivalent binary number of $(427)_8$
   a)100111010 b) 100111001 c)100010111 d) none
6. Find the octal number of $(1011111.0010111)_2$
   a)574.134 b)137.134 c)515.27 d) 571.134
7. What is the equivalent hexadecimal number of $(253.625)_{10}$?
   a)FD.A b) 1513.10 c) F13.A d) 15D.10
8. Convert $(BAD)_{16}$ into decimal number
   a)2898 b) 2889 c) 2998 d) 2989
9. Convert $(BED6)_{16}$ into binary number
   a) 1011111011010110 b) 10100110101 c) 1101010101010 d) none
10. Convert $(CAFE)_{16}$ into octal number
    a) 155476 b) 14547 c) 17558 d) 145376
11. Convert $(110101.10101)_2$ into hexadecimal number
    a)35.A8 b) 65.51 c) 53.108 d) 35.108
12. A particular number system having base B is given as $(V41)_B=5_{10.}$What is the value of B?
    a)5 b) 6 c)7 d)8

13. Find out the correct answer:

a)1 bit= 8byte b) 1byte =8 bit c) 1Nibble=4bit d) 1Byte =4 Nibble e) b & c

14. What is the value of base x for $(128)_{10}=(1003)_x$?

a)5 b)6 c)7 d)8

15. Consider $X=(54)_b$, where b is the base of the number system. If √x = 7 then what is the value of base b?

a)5 b)6 c)8 d)9

16. The equivalent 2's complement form of -8 is

a) 1001000 b) 1000 c) 01001 d)11000

17. How many number of Boolean expressions can be formed using 4 variable ?

a)32 b) 256 c)16 d)64K

18. 11001,1001 and 111001 correspond to the 2's complement representation of which one of the following sets of numbers?

a)-7,-1,-57 b) -6,-6,-6 c)-7,-7,-7 d)-25,-9,-57

19. What is decimal equivalent of BCD 11011.1100 ?

a) 22.0 b) 22.2 c) 20.2 d) 21.2

20. What is BCD representation of a decimal number 764?

a)010101010101 b)111110100 c)011101100100 d) none

21. The excess 3 code of decimal number 26 is

a) 0100 1001 b) 01011001 c) 1000 1001 d) 01001101

22. The excess-3 code of decimal 7 is represented by

a) 1100. b) 1001. c) 1011. d) 1010.

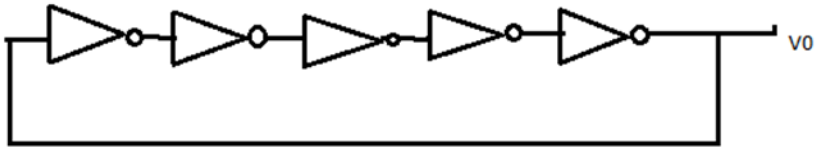
23. 8421 is a

a) Non-weighted code b) weighted code c) complementary code

24. The code where all successive numbers differ from their preceding number by single bit is

a) Binary code. b) BCD. c) Excess – 3. d) Gray

25. For the ring oscillator shown in figure, the propagation delay of each inverter is 100picoseconds.What is the fundamental frequency of the oscillator output?



a) 10Mhz b) 100Mhz c) 1Ghz d) 2Ghz

26. F=A'B'C' + A B' C' + AB' C + ABC' + ABC) . Express it as POS .

a) F = Π (1, 2, 3) b) F = Π (1, 2, 3, 4, 5)

c) F = Π (0, 5, 6) d) F = Π (0, 6, 7)

27. A bubbled AND gate is equivalent to

a) OR gate b) NAND gate c) NOR gate d) X-OR gate.

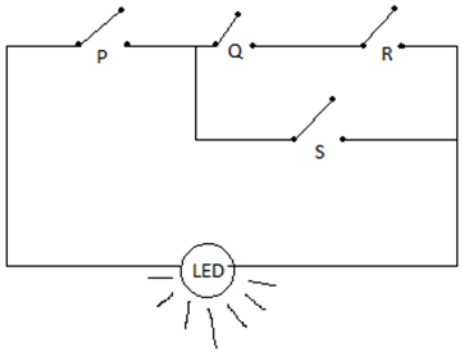
28.

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

What is the correct boolean expression of the truth table?

a)B(A+C)(A'+C') b) B(A+C')(A'+C) c) B'(A+C')(A'+C) d) B'(A+C)(A'+C')

29. Find the correct expression for the given switching circuits.



a)P+ (Q+R)S b) P(QR+S) c) P+QR+S d) None

30. Y= B (EXOR) B(EXOR) B……..n times, then the value of Y is

a)Zero, when n=even b) B, when n=even c) B, when n= odd d) a & c both

31.The minimum number of NAND gate to implement the Boolean function A+AB'+AB'C is:

a) 0 b)1 c)3 d)4

32.The range of signed decimal numbers that can be represented by 6bit 1's complement number is

a)-31 to + 31 b) -63 to +63 c) -64 to +63 d) -32 to + 31

Short Question [Type-2] **[Maximum marks: 2]**

1. Determine the 7's complement of the octal number 5674.
2. Find the 8's complement of an octal number 2675.
3. What is the one's complement representation of a binary number 101101?
4. What is the two's complement representation of a binary number 101101.011 & 110101.00100
5. Find out the $(EOB)_H$-$(ABF)_H$
6. Find the binary sum of 101101 & 110110
7. Subtract $(101101)_2$ from $(110110)_2$
8. Determine the value of

a) $(243)_8$+ $(547)_8$ b) $(743)_8$-$(562)_8$ c) $(ADD)_{16}$+$(BAD)_{16}$ d) $(9653)_{16}$ – $(2789)_{16}$

9. Subtract 17 from 45 using 2's complement method.
10. Subtract decimal number 22 from 17 using 8bit 2's complement method.

11. Subtract 26 from 14 using 1's complement method

12. Subtract 14 from 15 using 1's complement.

13. What will be the range of signed decimal numbers that can be represented by 6 bit 1's complement form?

14. 2's complement representation of a 16 bit number is FFFF. Its magnitude in decimal representation is what?

15. What will be the value of 2's complement of $(24)_{10}$?

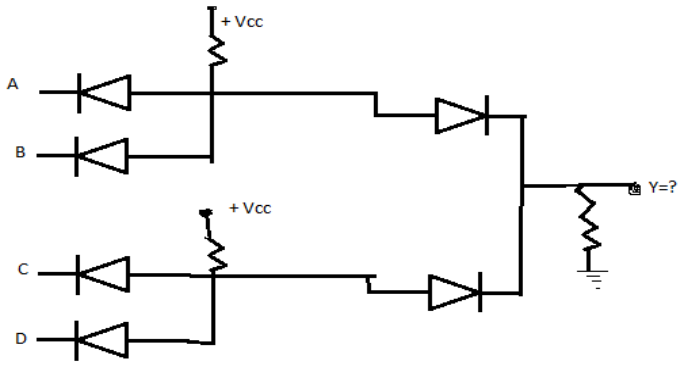
16. How many number of bytes are required to represent the decimal number 1856732 in packed BCD number ?

17. Find out the BCD addition of a) 24 + 26 b) 42+ 72 c) 46+ 64

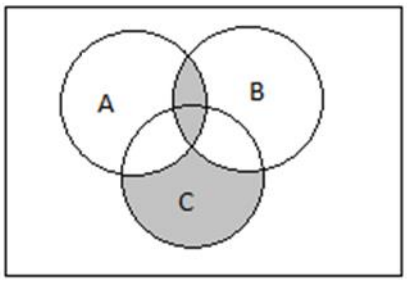
18. Design a circuit for : a) BCD to Excess-3 coder b) BCD to 7 segment decoder driver c) excess 3 code to BCD code using minimum number of logic gates.

19. Convert $(1011)_2$ to equivalent gray code and $(1101)_G$ to equivalent binary code.

20. For the given circuit ,find the output variable Y if input variables are A,B,C and D

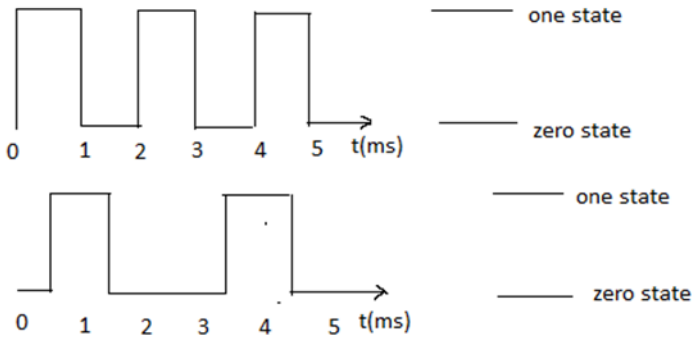


21. What is the Boolean expression for the shaded area in the Venn diagram?



22. How many NOR gates are required to implement (A+B).(C+D)?

23. The voltage waveforms shown in Fig.1 are applied at the inputs of 2-input AND and OR gates. Determine the output waveforms.



Subjective question [Type-3] **[Maximum marks: 3]**

1. State and prove Demorgan's laws.
2. Explain the different Boolean laws and theorems with example.
3. What are the differences between duality and complement?

Broad Question [Type-4] **[Maximum marks: 5]**

1.What are universal gates. Construct a logic circuit using NAND gates only for the expression x = A . (B + C).

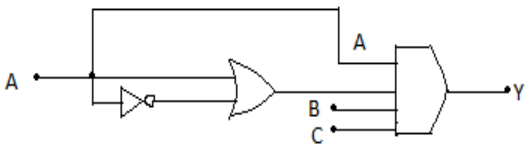
2. Simplify using k-map in SOP form : f (A, B, C, D) =∑m(1, 2, 4, 5,9,10) + ∑d (6,7,8,13)

3. Simplify the function using K-map and implement the result in AND –OR logic:

F(A,B,C,D)= ∑m(0,1,2,4,5,6,8,9,12,13,14)

4. What will be the output expression F, where F is high if and only if the majority of inputs are high?

5. What is the Boolean expression for the output of the logic circuit?



6. Two products are sold from a vending machine, which has two push buttons P1 and P2 .When a button is pressed ,the price of the corresponding product is displayed in a 7- segment display.

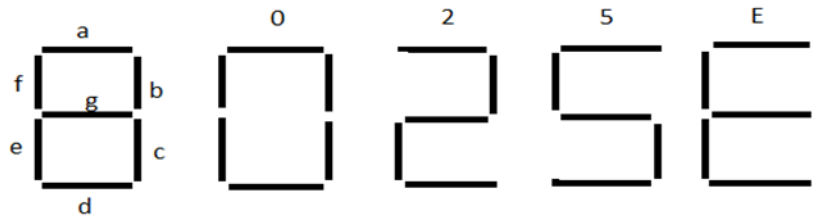
If no button are pressed, 0 is displayed, signifying Rs.0/-

If only P1 is pressed,2 is displayed, signifying Rs.2/-

If only P2 is pressed,5 is displayed, signifying Rs.5/-

If both P1 and P2 are pressed ,E is displayed, signifying error

The names of the segments in the 7 segment display and the glow of display for 0,2,5,E are shown below.



Consider:

i) Push button pressed / not pressed is equivalent to logic 1/0 respectively

ii) A segment glowing/not glowing in display is equivalent to logic 1/0 respectively.

If segment a to g are considered as functions of P1 and P2,then which of the following is correct?

a)g=P1'+P2,d=c+e b) g=P1+P2,d=c+e c) g=P1'+P2,e=b+c d) g=P1+P2,e=b+c

7. Simplify the following Boolean function:

i)AB + B(B + C') + B'C ii) C'F + F(A + B') + C iii)A+A'B+A'B'C+A'B'C'D + A'B'C'D'E+…….

Question Paper Details					
Course	**Stream**	**Semester**	**Subject**	**Paper Code**	**Chapter**
B.TECH	**ECE**	**4th**	**Digital Electronics & Integrated Circuits**	**EC-402**	**2 Combinational circuits,Memory Systems**

Paper Setter Details			
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MCQ [Type-1] **[Maximum marks: 1]**

1. A serial adder requires

a) one half adder b) two full adders c) one full adder d) one multiplexer

2.The final carry output equation of carry look ahead adder is

a)$C_{n+1}=P_nC_n+G_n$ b) $C_{n+1}=P_n+C_nG_n$ c) $C_n=P_n+C_nG_n$ d) $C_n=P_nC_n+G_n$

3. If A and B are the inputs of a half adder, the sum is given by

a) A AND B b) A OR B c) A XOR B d) A EXOR B

4. Half-adders have a major limitation in that they cannot

a) Accept a carry bit from a present stage b) Accept a carry bit from a next stage

c) Accept a carry bit from a previous stage d) None of the Mentioned

5. The difference between half adder and full adder is

a) Half adder has two inputs while full adder has four inputs

b) Half adder has one output while full adder has two outputs

c) Half adder has two inputs while full adder has three inputs

d) All of the Mentioned

6. The output of Full adder is represented as

a)Sum=∑m(1,2,4,7),Carry=∑m(3,5,6,7) b) Sum=∑m(1,2,4,7),Carry= AB+(A EXOR B)C

c)Sum=A (EXOR) B (EXOR) C, Carry=∑m(3,5,6,7) d) all

7. To make a full adder we need

a)EXOR gate=2,AND gate=2, OR gate=1 b) EXOR gate=3,AND gate=2, OR gate=1

c) EXOR gate=2,AND gate=3, OR gate=1 d) EXOR gate=1,AND gate=2, OR gate=3

8. A decoder with enables input can be used as

a) encoder b) demultiplexer c) comparator d) decoder

9. Multichannel signal can be transmitted through a single channel by using

a)encoder b) demultiplexer c) comparator d) multiplexer

10. The number of 2 to 4 line decoder are used to make a 4 to 16 line decoder is

a) 4 b) 5 c)6 d)7

11. The number of 2X1 MUX and 4x1 to make a 256X1 MUX is

a) 6,16 b) 255,85 c)58,552 d) 64,16

12. How many possible outputs would a decoder have with a 6-bit binary input?

a) 32 b) 64 c) 128 d) 16

13. A 4:16 decoder can be constructed (with enable input) by:

a)using four 2:4 decoder b) using five 2:4 decoder c) using two 3:8 decoder

14. Parity check bit coding is used for

a) Error correction b) Error detection c) Error correction and detection d) None of the above

15.The memory ,which is ultraviolet erasable and electrically programmable is

a)RAM b)EEROM c)PROM d) EPROM

16. A 1-bit full adder takes 20ns to generate carry out bit and 40ns for the sum bit.What is the maximum rate of addition per second when four 1bit full adder are cascaded?

a)10^7 b) $1.25x10^7$ c) $6.25x\ 10^6$ d) 10^5

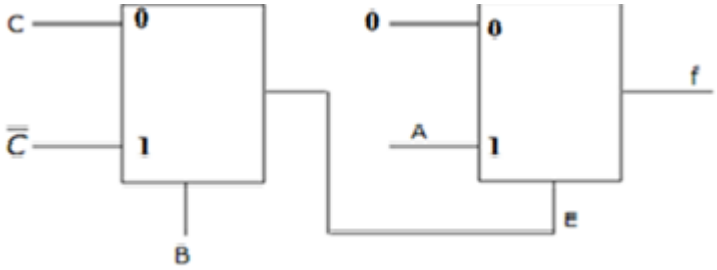
17. What is the number of select lines required in a single input and n output DEMUX?

a) 2 b) n c) $\log_2 n$ d) 3

18. A 4:16 decoder can be constructed (with enable input) by:

a)using four 2:4 decoder b) using five 2:4 decoder c) using two 3:8 decoder

19. What will be the output function :



a)AB'C+ABC' b)ABC+AB'C' c)A'BC+A'B'C' d) A'B'C+A'BC'

20. What are the minimum number of 2:1 MUX required to generate a 2 input AND gate and a 2 input EX-OR gate?

a) 1,2 b) 2,1 c) 3,1 d)1,3

21. Four memory chips of 16x4 size have their address buses connected together. This system will be of size

a)64x4 b)16x16 c)32x8 d)256x1

22.How many address inputs and data inputs are required for a16Kx12 memory

a)12,12 b)16,12, c)14,12 d)16,16

23. Which one is right for PAL:

a)AND array is programmable , OR array is fixed b) AND array is fixed , OR array is programmable

c)Both are fixed d) Both are programmable

Short Question [Type-2] [Maximum marks: 2]

1.What are differences between combinational and sequential circuits?

2. Explain a 2 bit comparator with diagram.

3. Design a half adder using 2 to 4 decoder with additional logic gates, if required.

4. Design a half subtractor using 2 to 4 decoder with additional logic gates, if required.

5. How many minimum number of 2:1 MUX are required for implementing the Half Adder and Half Subtractor?

Subjective question [Type-3] **[Maximum marks: 3]**

1.Explain the operation of Full adder.

2. Design a Full adder using 3 to 8 decoder with additional logic gates, if required.

3. Design a Full subtractor using 3 to 8 decoder with additional logic gates, if required.

4. Write a short note on: Even Parity Generator and Checker

5. Explain and design a look ahead carry adder.

6. What is parallel adder? Draw and explain block diagram for 4 bit parallel adder. 7. Write the differences between ROM, RAM, EPROM, EEROM.

8. Write a short note on: EPROM

9. Write the differences between SRAM and DRAM.

10. Write the differences between RAM and ROM.

Broad Question [Type-4] **[Maximum marks: 5]**

1. Design a full adder with two half adders and explain it.

2. Design a full subtractor with two half subtractor and explain.

3. Design a full subtractor using decoder and necessary gates.

4. Design a Full adder using necessary Multiplexer.

5. Design a Full subtractor using necessary Multiplexer.

6. Implement f(A,B,C)=∑m(0,1,4,6,7) using MUX,taking A,B as select line.

7. Implement F(A,B,C,D)=∑m(0,1,3,5,7,8,9,11,12,14) in Multiplexer.

8. Implement F(A,B,C)= A+BC in a Multiplexer.

9. Explain how a Multiplexer is used as a universal circuit.

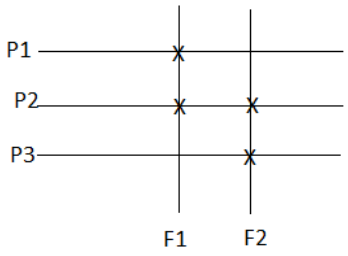
10. Implement the following Boolean equations using PLA device :F=∑m(1,3,7,11,13)

11. Implement BCD to Excess-3 code conversion using ROM .

12. It is desired to generate the following three Boolean functions:

i) F1: a b’ c+ a’ b c’+ b c ; ii) F2= a b’ c + a b +a’ b c’

By using an OR gate array as shown below, where P1 to P3 are the product terms in one or more of the valuables a, a' ,b ,b' ,c, c'



Find out the terms P1,P2 and P3

13.What is a digital comparator? Explain the working of a 4-bit digital comparator .

14. Implement the logic function f=∑m(0,1,3,5,7) by using ROM.

Question Paper Details					
Course	**Stream**	**Semester**	**Subject**	**Paper Code**	**Chapter**
B.TECH	**ECE**	**4th**	**Digital Electronics & Integrated Circuits**	**EC-402**	**3 Sequential Circuits**

Paper Setter Details			
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MCQ [Type-1] **[Maximum marks: 1]**

1. Which flip-flop acts as a buffer?

a) D flip-flop b) SR flip-flop c) T flip-flop d) JK flip-flop

2. The characteristic equation of T flip-flop is

a) $Q_{n+1} = T'Q_n + TQ_n'$ b) $Qn+1 = TQ_n + T'Q_n'$ c) $Q_{n+1} = TQ_n$ d) $Q_{n+1} = TQ_n'$

3. Master slave f/f has the characteristic that

a)change in the input immediately reflected in the output

b)change in the output occurs when state of the master is affected

c) change in the output occurs when state of the slave is affected

d)both the master and slave states are affected at the same time.

4. Choose the correct one by matching the item of Gr-1 and Gr-2

Gr-1	Gr-2
A. Shift register	1. Frequency division
B. Counter	2. Addressing in memory chips
C. Decoder	3. Serial to parallel data conversion

a)A-3,B-2,C-1 b)A-3,B-1,C-2 c)A-2,B-1,C-3 d)A-1,B-2,C-3

5.The number of flip-flops required for a MOD-10 ring counter is

a) 4 b) 10 c) 5 d) none of these

6. The number of flip-flops required for a MOD-10 Johnson counter is

a) 4 b) 10 c) 5 d) none of these

7. Latch is a memory cell of

a) 1 bit b) 2 bit c) 3 bit d) none of these .

8.The initial output Q of SR f/f is 0.It changes to 1,when clock pulse is applied.The input S-R will be:

a) S=0,R=0 b) S=0,R=1 c) S=1,R=0 d) S=1,R=1

9.Mod-2 counter followed by Mod -5 counter is

a) Mod -7 counter b) Mod -3 counter c) Decade counter d) Mod -9 counter

10.4 bit Ripple counter counts upto

a)4 b) 12 c) 16 d) 15

11.Master slave f/f is to

a)increase clock rate b)reduce power dissipation

c)eliminate race around condition d) improve reliability

12. The output frequency of a decade counter clocked from a 50khz signal is

a)50Khz b)500Khz c)5Khz d)25 Khz

13. 10 MHZ signal is applied to a MOD-5 Counter followed by MOD-8 counter. The output frequency will be

a) 10 kHz b) 2.5 kHz c) 5 kHz d) 25 kHz.

14. An SR latch is

a)Combinational circuit b) sequential circuit c) one bit memory element

15. Race around occurs

a) when J=K=0 b) J=K=1 c) J=0 K=1 d) J=1,K=0

16. The condition to avoid race around is

a) $T_{clk} < t_{pw} < t_{pdff}$ b) $t_{pdff} < T_{clk} < t_{pw}$ c) $t_{pw} < t_{pdff} < T_{clk}$

17. The slave F/F of Master Slave F/F is

a) level triggered b) edge triggered c) no triggered

18. A single bit memory device is

a)register b) Flip flop c) counter d)none

19. The modulus of a counter is

a) actual number of states in its sequence b) maximum number of states

c) number of flip-flop d) number of clock pulse

20. A decade counter counts upto

a)9 b) 10 c) 11 d) 12

21. How many Flip-Flops are required for mod–16 counter?

a) 5 b) 6 c) 3 d) 4

Short Question [Type-2] **[Maximum marks: 2]**

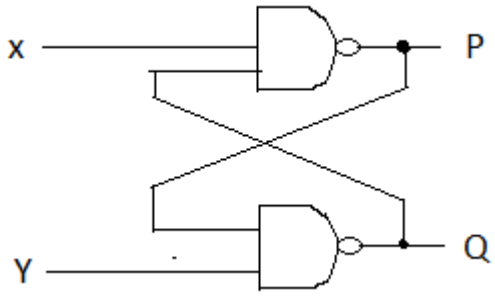
1. What is flip-flop ?

2. What are differences of Synchronous and asynchronous counter?

3.The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

X=0,Y=1 ; X=0,Y=0; X=1,Y=1

What will be the corresponding stable P,Q outputs ?



4. Explain race around condition of J-K flip-flop.

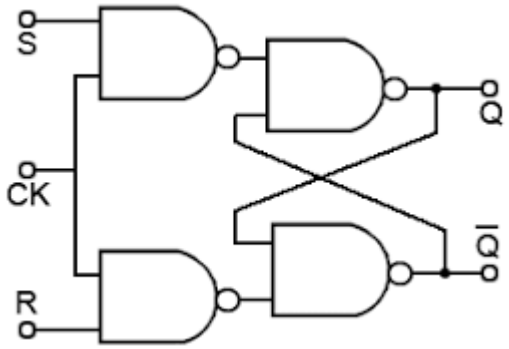
5. What do you mean by the asynchronous inputs of a flip-flop ?

6. What is main differences between latch and flip-flop?

Subjective question [Type-3] **[Maximum marks: 3]**

1. Show how race around can be avoided.

2. Convert this flip flop into D – flip flop:



3. What is edge trigger flip-flop and why is it required ? What is differences between edge triggered and level triggered flip-flop?

4. Design a ripple counter with explaining the timing diagram.

5. Design a Ring counter with 4 state.

6.Expalin the working principle of Parallel-In-Serial-Out register.

7.Design a bidirectional shift register with diagram.

9. Explain JK flip flop with a neat diagram.

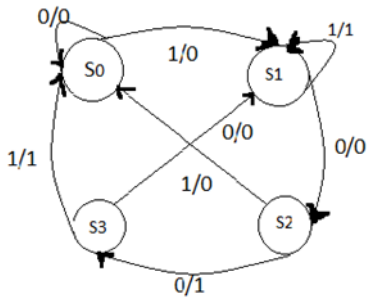
10. Explain how a counter can be used as frequency divider with a proper example.

Broad Question [Type-4] **[Maximum marks: 5]**

1. Convert S-R flip-flop to J-K and R flip-flop respectively.

2. Design a MOD-6 synchronous counter using JK flip flop and D flip-flop.

3. Design a sequential circuit using D flip-flop that implements the following state diagram:



4. What is a Shift Register? What are its various types? List out some applications of Shift Register.

5. Explain how a shift register can be used as a ring counter giving the wave forms.

6. Realize a 4 bit ring counter and develop the state table.

7. Design a 4bit twisted ring counter and find out the number of unused state.

Question Paper Details					
Course	**Stream**	**Semester**	**Subject**	**Paper Code**	**Chapter**
B.TECH	**ECE**	**4th**	**Digital Electronics & Integrated Circuits**	**EC-402**	**4 ADC AND DAC Techniques, Logic families**

Paper Setter Details			
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MCQ [Type-1] **[Maximum marks: 1]**

1.Which family has the better noise margin ?

a)ECL b) DTL c) MOS d) TTL

2. Which family has the better speed ?

a) ECL b) DTL c) TTL d) MOS

3.The faster ADC is

a)Dual slope type b) SAR type c) counter type d) none

4.The faster logic gate family is

a)CMOS b) ECL c) TTL d) RTL

5. A Darlington emitter –follower circuit is sometimes used in the output stage of a TTL gate in order to

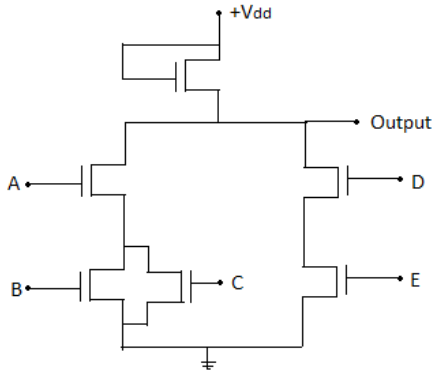
a) increase its I_{OL} b) reduce its I_{OH} c) increase its speed of operation d) reduce power dissipation

6. Commercially available ECL gears use two ground lines and one negative supply in order to

a) reduce power dissipation b) increase fan out

c) reduce loading effect d) eliminate the effect of power line glitches or the biasing circuit

7. An NMOS circuit is shown in the above figure.The logic function for the output is



a)(A+B)'C+D'E' b) (AB+C')(D'+E) c)A(B+C)'DE d)(ABCD)'

8. What will be the value of current in DAC circuit using inverted OP-AMP,where V_R=10V and R=10Kohm

a) 31.25 µA b) 62.5 µA c) 125 µA d)250 µA

9. A 10 bit A/D converter is used to digitize an analog signal in the 0 to 5V range.What is the approximate value of the maximum peak to peak ripple voltage that can be allowed in the dc supply voltage?

a)100mV b) 50mV c) 25mV d) 5 mV

10. The resolution of a 4 bit counting ADC is 0.5 V.For an analog input of 6.6 volts,the digital output of the ADC will be

a)1011 b)1101 c) 1100 d) 1110

11. An 8bit successive approximation analog to digital converter has full scale reading of 2.55 V and its converstion time for an analog input of 1V is 20 µs.The conversion time for a 2V input will be

a)10µs b) 20 µs c) 40 µs d)50 µs

12. The number of comparators in a 4 bit flash ADC is

a)4 b) 5 c) 15 d) 16

13.The output of TTL gate is taken from a BJT in

a)totem pole and common collector configuration

b)either totempole or open collector configuration

c)common base configuration

d) common collector configuration

14. What is the full form of TTL?

a) Tansient Transistor Log b) Transistor Transistor Logic c) Tripple Transistor Logic d) Tristate Transistor Logic

Short Question [Type-2] **[Maximum marks: 2]**

1.What is the largest value of output from an 8-bit DAC that produces 1.0V for a digit input of 00110010?

2. Define resolution of a DAC wih an example.

3. Define the terms a) Set up time b) Hold time C) fan out d) Power dissipation

Subjective question [Type-3] **[Maximum marks: 3]**

1. Write a short note on:

a)R2R Ladder type DAC b) TTL c) Dual slope ADC d) Successive approximation ADC e)Counter type ADC

2. A 6 bit DAC has step size 50mV. Determine a full scale output voltage and resolution.

3. Describe CMOS inverter and state advantages of CMOS.

4. A 6-bit Dual Slope A/D converter uses a reference of –6V and a 1 MHz clock. It uses a fixed count of 40 (101000). Find Maximum Conversion Time.

5. Define fan out. Which factor is responsible for the limit of fan out in TTL circuits?

6. Implement the function (AB+CD)'

Broad Question [Type-4] **[Maximum marks: 5]**

1. Draw the circuit diagram of a two input TTL NAND gate and label component values and write the function table.

2. Implement F= (A+B)(C+D) using CMOS, NMOS and PMOS.

3. With the help of R-2R binary network, explain the working of a 3-bit D/A converter and derive

an expression for the output voltage.

4.Explain the operation of ECL with diagram.

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