TECHNO INDIA – BATANAGAR
(DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING)
QUESTION BANK- 2018

Paper Setter Detail			
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QUESTION PAPER DETAILS					
Course	**Stream**	**Semester**	**Subject**	**Paper Code**	**Module**
B. Tech	**ECE**	**7th**	**Microelectronics & VLSI Designs**	**EC-702**	**1.Introduction to VLSI Design**

MCQ: Type-1 (Maximum marks to be allotted =1)

1. MOS transistor
   A. Has only one p-n junction.
   B. Has only two electrodes.
   C. Gate electrode is in direct contact with silicon.
   D. Conducts when sufficient voltage is applied to gate electrode.
2. The polarity of the inversion layer in a MOSFET is same as
   A. Charge on gate electrode
   B. Minority carriers in the drain
   C. Majority carriers in the substrate
   D. Majority carriers in the source
3. NMOS are better than PMOS because
   A. Better noise immunity
   B. Faster
   C. TTL compatible
   D. Better drive capability
4. MOSFETs can be operated at higher frequencies as compared to BJTs because
   A. MOSFETs have higher input impedance
   B. MOSFETs are voltage controlled
   C. MOSFETs have positive temperature coefficients
   D. Minority carriers storage time is absent in MOSFETs
5. Consider two statements
   I. NMOS requires reverse voltage for turn off.
   II. PMOS requires forward gate voltage for turn off.
   A. I and II are correct
   B. I is correct and II is wrong
   C. I is wrong and II is correct
   D. I and II are wrong

6. The region of operation of device for V_{DS}=5V
    A. Cut-off
    B. Saturation
    C. Triod
    D. None of the above
7. What is the function of SiO_2 layer in MOSFETS
    A. To provide high input resistance
    B. To increase current carrier
    C. To provide high output resistance
    D. both a and c
8. Among the following which one has the greatest gate integration capacity?
    A. FPGA
    B. CPLD
    C. PLD
    D. ASIC
9. In a PAL
    A. Only AND array is programmable
    B. Only OR array is programmable
    C. Both A and B
    D. Macro cell is the building block
10. Which design is more efficient?
    A. Pull up and pull down design
    B. TG design
    C. Pre charge and evaluate logic

Short Question: <u>Type-2</u> (Maximum marks to be allotted =2)

1. Design a half subtractor circuit using PLA.
2. What is modularity of VLSI design?
3. What is locality of VLSI design?
4. Which current is dominant in MOSFET? Drift or diffusion?
5. What is subthreshold conduction and what accounts for it?

Subjective Question: <u>Type-3</u> (Maximum marks to be allotted =3)

1. Design a PROM which takes 3 binary bits as input and generates the output which is square of the input.
2. Classify the different type of ASIC design.
3. Why Silicon is chosen normally for fabrication of MOSFET?
4. Compare FPGA and CPLD.
5. What are the limitation of IC's?

Broad Question: <u>Type-4</u> (Maximum marks to be allotted =5)

1. Design the following circuit using PAL,PLA,PROM.

2. What is “divide and conquer method”? Explain.
3. Write short notes on the following:
    A. CPLD.
    B. FPGA.
    C. Programmable Logic Array.
    D. Y-chart of VLSI design flow.
4. How do you expect the gate source capacitance of a MOSFET to vary with gate source voltage? Explain your answer.
5. What is the main constructional difference between a MOSFET and a BJT ?What effect do they have on the current conduction mechanism of a MOSFET?

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B. Tech	**ECE**	**7th**	**Microelectronics & VLSI Designs**	**EC-702**	**2.Micro-electronic Processes for VLSI Fabrication**

MCQ: <u>Type-1</u> (Maximum marks to be allotted =1)

1. The output of physical design is
    A. Layout
    B. Mask
    C. RTL
    D. Circuit Design
2. Czochralski Process is used to form
    A. Wafer
    B. Ingot
    C. IC
    D. None of these
3. The difference between a depletion load MOSFET and Enhancement MOSFET only is the absence of
    A. Insulated gate
    B. Electrons
    C. Induced channel
    D. None of these
4. Material used for the fabrication of Gate in modern MOSFET
    A. Highly pure Si
    B. Highly doped polysilicon
    C. Highly pure SiO_2
    D. None of these
5. Twin – Tube process is widely used for fabrication of
    A. CMOS
    B. PMOS

C. NMOS
D. None of these

6. Epitaxial growth in IC chip
    A. Growth from liquid phase
    B. Can be p type only
    C. Growth from gas phase
    D. Can be n type only
7. Registers are fabricated in the monolithic IC process during
    A. Exitaxial growth
    B. Base diffusion
    C. Emitter and collector diffusion
    D. Base or emitter diffusion
8. Ion implantation is done
    A. At lower temperature than diffusion
    B. At higher temperature than diffusion
    C. Almost at same temperature than diffusion
9. In a simple n-well CMOS fabrication technology
    A. The NMOS is created in the p type substrate
    B. The NMOS is created in the n type substrate
    C. Both NMOS and PMOS are created in the p type substrate
    D. Both NMOS and PMOS are created in the n type substrate
10. A negative photoresist becomes
    A. Less soluble in developer's solution
    B. More soluble in developer's solution
    C. Positive photoresist under UV exposure
    D. None of these

Short Question: Type-2 (Maximum marks to be allotted =2)

1. What is isolation? What are the different ways to obtain it?
2. What is oxidation?
3. With a suitable diagram briefly describe the p-well fabrication process of a CMOS inverter.
4. Distinguish between diffusion and ion-implantation technique.
5. What is meant by Molecular Beam Epitaxy (MBE)?

Subjective Question: <u>Type-3</u> (Maximum marks to be allotted =3)

1. What are the different process steps a typical IC fabrication process consists of?
2. What is evaporation and sputtering?
3. Describe the photo-lithography process.
4. Describe the N-well CMOS fabrication process.
5. What is lithography? Mention various types of lithography used in VLSI.

Broad Question: Type-4 (Maximum marks to be allotted =5)

1. What do you mean by 'Lamda Rule' & 'Micron Rule' ?Draw the layout & Schematic diagram of a static CMOS NAND/NOR gate & identify the corresponding components in the two drawing.
2. Describe the Fick's law for Diffusion process. What do you mean by isotropic & anistropic etching processes?
3. Describe the CMOS fabrication process with proper diagram.
4. What are prebake and postbake in lithography? What are the characteristics of exposure tools used in lithography?
5. Explain the following dominant CMOS fabrication process with neat diagrams.
    A. P-well process
    B. N-well process
    C. Twin tube process
    D. Silicon on insulator

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Course	**Stream**	**Semester**	**Subject**	**Paper Code**	**Module**
B. Tech	**ECE**	**7th**	**Microelectronics & VLSI Designs**	**EC-702**	**3.CMOS for Digital VLSI Circuits**

MCQ: Type-1 (Maximum marks to be allotted =1)

1. The threshold voltage of an enhancement transistor is
    A. Greater than 0V
    B. Less than 0V
    C. Equal to 0V
    D. None of these
2. The MOS device can be used as a resistor in
    A. Saturation region
    B. Linear region
    C. Subthreshold condition
    D. Superthreshold condition
3. A MOS diode is not a component of
    A. Level translator
    B. Current mirror
    C. Current sink
    D. Rectifier circuit
4. When a MOSFET is in saturation region, the effective channel length increases
    A. With decreasing V_{GS}
    B. With increasing V_{GS}

C. With increasing V_{DS}
D. With decreasing V_{DS}

5. How many transistors are required to implement the function F=AB+C(A+B) using CMOS logic?
   A. 10
   B. 6
   C. 8
   D. 12
6. How many transistors are required to implement a 2:1 MUX using TG?
   A. 4
   B. 6
   C. 8
   D. 10
7. The advantage of CMOS TG over single pass transistor logic is?
   A. Low transfer time
   B. No threshold voltage drop
   C. Both A & B
   D. Single phase clock is required
8. Dynamic logic circuits require periodic clock signals in order to
   A. Improve performance
   B. Synchronization
   C. Increase density
   D. Charge refreshing
9. The operation of dynamic logic circuit depends on
   A. Temporary storage of charge in parasitic node capacitance
   B. Non over lapping clocks
   C. Low power dissipation
   D. None of these
10. The disadvantage of CMOS inverter is
    A. Complex fabrication
    B. Space requirement
    C. Poor noise margin
    D. Latch-up

Short Question: Type-2 (Maximum marks to be allotted =2)

1. What are the disadvantages of dynamic logic?
2. What is clock gating?
3. What is metastability? When/Why it will occur?
4. What is clock skew?
5. What is glitch?

Subjective Question: Type-3 (Maximum marks to be allotted =3)

1. Design a clocked CMOS circuit that implements the function F= (A.B+C)'
2. Implement the logic function F= (A.B+C.A)' using smallest number of transistor in dynamic logic.
3. What are the advantages of dynamic logic over static logic?
4. What is clock distribution network?
5. Draw the NOR gate based JK latch circuit and it's AOI implementation.

Broad Question: Type-4 (Maximum marks to be allotted =5)

1. Implement the two logic functions given by F= A+B+C and G= A+B+C+D
    A. Using cascaded dynamic logic gates
    B. Using NP CMOS logic
2. Draw the circuit diagram of 2 input NOR gate based SR latch with depletion load NMOS transistor. Compare the performance with CMOS NOR gate based SR latch.
3. Explain about setup time and hold time. What will happen if there is setup time and hold time violation and how to overcome this?
4. Is it possible to reduce clock skew to zero? Explain your answer.
5. Explain why it is necessary to introduce a feedback path in a sequential circuit. Is it sufficient that a circuit with a feedback path will be a sequential circuit.

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Course	**Stream**	**Semester**	**Subject**	**Paper Code**	**Module**
B. Tech	**ECE**	**7th**	**Microelectronics & VLSI Designs**	**EC-702**	**4.Analog VLSI Circuits**

MCQ: Type-1 (Maximum marks to be allotted =1)

1. Switched capacitor circuits are
    A. Continuous in amplitude and time
    B. Discrete in amplitude and time
    C. Continuous in amplitude and discrete in time
    D. Discrete in amplitude and continuous in time
2. For a MOS resistor
    A. $r_{ds} \infty (V_{GS}-V_{th})^2$
    B. $r_{ds} \infty (V_{GS}-V_{th})$
    C. $r_{ds} \infty 1/(V_{GS}-V_{th})^3$
    D. $r_{ds} \infty 1/(V_{GS}-V_{th})$
3. For a differential amplifier,differential trans-conductance is given by
    A. $g_m \infty I_D^{3/2}$
    B. $g_m \infty I_D^{1/2}$
    C. $g_m \infty I_D$
    D. $g_m \infty I_D^2$

4. Unit of $\mu_n C_{ox}$ is
    A. A/V^2
    B. V^2
    C. Ω^{-1}
    D. A^2/V^2
5. Typical value of sub-threshold slope is
    A. 100 mV/decade
    B. 50 mV/decade
    C. 60 mV/decade
    D. 90 mV/decade
6. In a saturated MOSFET ,with increasing V_{DS} ,channel length
    A. Increases
    B. Decreases
    C. Remain same
    D. May increase or decrease
7. In which device at zero gate voltage the channel already exist?
    A. Depletion type MOSFET
    B. CMOS device
    C. Enhancement type MOSFET
8. The potential at which the inversion layer dominates the substrate behaviour is
    A. Pinch-off voltage
    B. Cut-off voltage
    C. Threshold voltage
9. The overlap capacitance is
    A. Voltage dependent
    B. Voltage independent
    C. None of these
10. The condition where the majority carrier concentration is greater near the SiO_2 interface compared to the bulk in the MOSFET is called
    A. Accumulation
    B. Depletion
    C. Inversion

Short Question: Type-2 (Maximum marks to be allotted =2)

1. Explain channel length modulation.
2. What is scaling of MOSFET?
3. What is current sink?
4. What is current source?
5. How can resistance of a current source/sink be improved?

Subjective Question: <u>Type-3</u> (Maximum marks to be allotted =3)

1. What is an ideal op-amp?
2. Draw the block diagram of 2 stage CMOS OPAMP.

3. What is switched capacitor filter?
4. Design the 1^{st} and 2^{nd} order switched capacitor low – pass filters.
5. Describe the operation of MOSFET differential amplifier.

Broad Question: <u>Type-4</u> (Maximum marks to be allotted =5)

1. What is current mirror? Explain with proper circuit diagram.
2. Find the "input common mode range" and "output swing" of a 2 stage CMOS OPAMP.
3. How can you realize the resistor using switched capacitor circuits?
4. What do you mean by Series – Parallel switched capacitor circuit? Describe briefly.
5. Describe the different types of Switched Capacitor Integrator Circuit. Describe the drawbacks of discrete-time integrator. How do you solve this drawback?
6. Write short notes on
    A. Folded – cascade amplifier
    B. MOS capacitance
    C. Switched capacitor